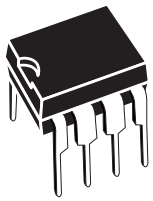
M93C86, M93C76, M93C66
M93C56, M93C46

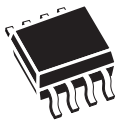
16 Kbit, 8 Kbit, 4 Kbit, 2 Kbit and 1 Kbit (8-bit or 16-bit wide) MICROWIRE® serial access EEPROM

Features

- Industry standard MICROWIRE bus
- Single supply voltage:
  - 4.5 V to 5.5 V for M93Cx6
  - 2.5 V to 5.5 V for M93Cx6-W
  - 1.8 V to 5.5 V for M93Cx6-R
- Dual organization: by word (x16) or byte (x8)
- Programming instructions that work on: byte, word or entire memory
- Self-timed programming cycle with auto-erase: 5 ms
- READY/$\overline{\text{BUSY}}$ signal during programming
- 2 MHz clock rate
- Sequential read operation
- Enhanced ESD/latch-up behavior
- More than 1 million write cycles
- More than 40 year data retention
- Packages
  - ECOPACK® (RoHS compliant)



PDIP8 (BN)



SO8 (MN)
150 mil width

TSSOP8 (DW)
169 mil width

UFDFPN8 (MB)
2 x 3 mm (MLP)

Table 1. Product list

Reference	Part number	Reference	Part number
M93C86	M93C86	M93C56	M93C56
	M93C86-W		M93C56-W
	M93C86-R		M93C56-R
M93C66	M93C66	M93C46	M93C46
	M93C66-W		M93C46-W
	M93C66-R		M93C46-R
M93C76	M93C76		
	M93C76-W		
	M93C76-R		

1 Description

The M93C86, M93C76, M93C66, M93C56 and M93C46 are electrically erasable programmable memory (EEPROM) devices. They are accessed through a Serial Data input (D) and Serial Data output (Q) using the MICROWIRE bus protocol.

Figure 1. Logic diagram

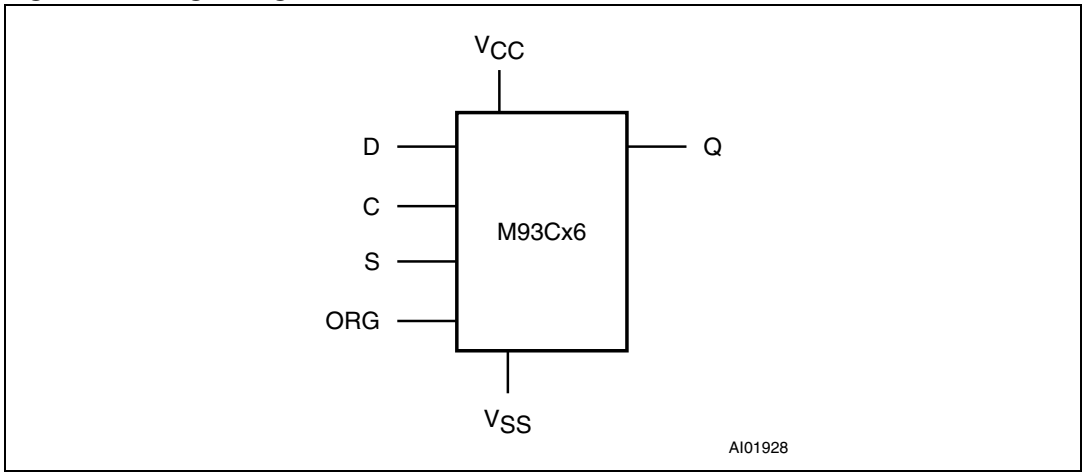


Table 2. Signal names

Signal name	Function	Direction
S	Chip Select	Input
D	Serial Data input	Input
Q	Serial Data output	Output
C	Serial Clock	Input
ORG	Organisation Select	Input
V_{CC}	Supply voltage	
V_{SS}	Ground	

The memory array organization may be divided into either bytes (x8) or words (x16) which may be selected by a signal applied on Organization Select (ORG). The bit, byte and word sizes of the memories are as shown in *Table 3.*

Table 3. Memory size versus organization

Device	Number of bits	Number of 8-bit bytes	Number of 16-bit words
M93C86	16384	2048	1024
M93C76	8192	1024	512
M93C66	4096	512	256
M93C56	2048	256	128
M93C46	1024	128	64

The M93Cx6 is accessed by a set of instructions, as summarized in *Table 4.*, and in more detail in *Table 5.* to *Table 7.*).

Table 4. Instruction set for the M93Cx6

Instruction	Description	Data
READ	Read Data from Memory	Byte or Word
WRITE	Write Data to Memory	Byte or Word
WEN	Write Enable	
WDS	Write Disable	
ERASE	Erase Byte or Word	Byte or Word
ERAL	Erase All Memory	
WRAL	Write All Memory with same Data	

A Read Data from Memory (READ) instruction loads the address of the first byte or word to be read in an internal address register. The data at this address is then clocked out serially. The address register is automatically incremented after the data is output and, if Chip Select Input (S) is held High, the M93Cx6 can output a sequential stream of data bytes or words. In this way, the memory can be read as a data stream from eight to 16384 bits long (in the case of the M93C86), or continuously (the address counter automatically rolls over to 00h when the highest address is reached).

Programming is internally self-timed (the external clock signal on Serial Clock (C) may be stopped or left running after the start of a Write cycle) and does not require an Erase cycle prior to the Write instruction. The Write instruction writes 8 or 16 bits at a time into one of the byte or word locations of the M93Cx6. After the start of the programming cycle, a Busy/Ready signal is available on Serial Data Output (Q) when Chip Select Input (S) is driven High.

An internal Power-on Data Protection mechanism in the M93Cx6 inhibits the device when the supply is too low.

10 Maximum rating

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 8. Absolute maximum ratings

Symbol	Parameter		Min.	Max.	Unit
T_A	Ambient operating temperature		–40	130	°C
T_{STG}	Storage temperature		–65	150	°C
T_{LEAD}	lead temperature during soldering	PDIP		260(1)	
		other packages	See note (2)		°C
V_{OUT}	Output range (Q = V_{OH} or Hi-Z)		–0.50	V_{CC}+0.5	V
V_{IN}	Input range		–0.50	V_{CC}+1	V
V_{CC}	Supply voltage		–0.50	6.5	V
V_{ESD}	Electrostatic discharge voltage (human body model)(3)		–4000	4000	V

1. T_{LEAD}max must *not* be applied for more than 10 s.
2. Compliant with JEDEC Std J-STD-020C (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
3. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω).

11 DC and AC parameters

This section summarizes the operating and measurement conditions, and the dc and ac characteristics of the device. The parameters in the dc and ac characteristic tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 9. Operating conditions (M93Cx6)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	4.5	5.5	V
T_A	Ambient operating temperature (device grade 6)	–40	85	°C
	Ambient operating temperature (device grade 3)	–40	125	°C

Table 10. Operating conditions (M93Cx6-W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature (device grade 6)	–40	85	°C
	Ambient operating temperature (device grade 3)	–40	125	°C

Table 11. Operating conditions (M93Cx6-R)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.8	5.5	V
T_A	Ambient operating temperature (device grade 6)	–40	85	°C

Table 12. AC measurement conditions (M93Cx6)(1)

Symbol	Parameter	Min.	Max.	Unit
C_L	Load capacitance	100		pF
	Input rise and fall times		50	ns
	Input pulse voltages	0.4 V to 2.4 V		V
	Input timing reference voltages	1.0 V and 2.0 V		V
	Output timing reference voltages	0.8 V and 2.0 V		V

1. Output Hi-Z is defined as the point where data out is no longer driven.

Table 13. AC measurement conditions (M93Cx6-W and M93Cx6-R)(1)

Symbol	Parameter	Min.	Max.	Unit
C_L	Load capacitance	100		pF
	Input rise and fall times		50	ns
	Input pulse voltages	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input timing reference voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V
	Output timing reference voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V

1. Output Hi-Z is defined as the point where data out is no longer driven.

Figure 8. AC testing input output waveforms

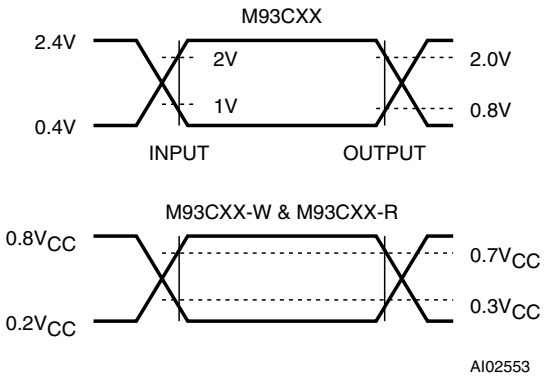


Table 14. Capacitance(1)

Symbol	Parameter	Test condition	Min	Max	Unit
C_{OUT}	Output capacitance	V_{OUT} = 0V		5	pF
C_{IN}	Input capacitance	V_{IN} = 0V		5	pF

1. Sampled only, not 100% tested, at T_A = 25 °C and a frequency of 1 MHz.

Table 15. DC characteristics (M93Cx6, device grade 6)

Symbol	Parameter	Test condition	Min.	Max.	Unit
I_{LI}	Input leakage current	0V ≤V_{IN} ≤V_{CC}		±2.5	µA
I_{LO}	Output leakage current	0V ≤V_{OUT} ≤V_{CC}, Q in Hi-Z		±2.5	µA
I_{CC}	Supply current	V_{CC} = 5 V, S = V_{IH}, f = 2 MHz, Q = open		2	mA
I_{CC1}	Supply current (Standby)	V_{CC} = 5 V, S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}, pin7 = V_{CC}, V_{SS} or Hi-Z		15	µA
V_{IL}(1)	Input low voltage	V_{CC} = 5 V ± 10%	–0.45	0.8	V
V_{IH}(1)	Input high voltage	V_{CC} = 5 V ± 10%	2	V_{CC} + 1	V
V_{OL}(1)	Output low voltage	V_{CC} = 5 V, I_{OL} = 2.1 mA		0.4	V
V_{OH}(1)	Output high voltage	V_{CC} = 5 V, I_{OH} = –400 µA	0.8V_{CC}		V

1. The input and output levels are compatible with TTL logic levels.

Table 16. DC characteristics (M93Cx6, device grade 3)

Symbol	Parameter	Test condition	Min.	Max.	Unit
I_{LI}	Input leakage current	$0V \le V_{IN} \le V_{CC}$		±2.5	µA
I_{LO}	Output leakage current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply current	V_{CC} = 5 V, S = V_{IH}, f = 2 MHz, Q = open		2	mA
I_{CC1}	Supply current (Standby)	V_{CC} = 5 V, S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}, pin7 = V_{CC}, V_{SS} or Hi-Z		15	µA
V_{IL}	Input low voltage	V_{CC} = 5 V ± 10%	–0.45	0.8	V
V_{IH}	Input high voltage	V_{CC} = 5 V ± 10%	2	V_{CC} + 1	V
V_{OL}	Output low voltage	V_{CC} = 5 V, I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output high voltage	V_{CC} = 5 V, I_{OH} = –400 µA	0.8 V_{CC}		V

Table 17. DC characteristics (M93Cx6-W, device grade 6)

Symbol	Parameter	Test condition	Min.	Max.	Unit
I_{LI}	Input leakage current	$0V \le V_{IN} \le V_{CC}$		±2.5	µA
I_{LO}	Output leakage current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply current (CMOS inputs)	V_{CC} = 5 V, S = V_{IH}, f = 2 MHz, Q = open		2	mA
		V_{CC} = 2.5 V, S = V_{IH}, f = 2 MHz, Q = open		1	mA
I_{CC1}	Supply current (Standby)	V_{CC} = 2.5 V, S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}, pin7 = V_{CC}, V_{SS} or Hi-Z		5	µA
V_{IL}	Input low voltage (D, C, S)		–0.45	0.2 V_{CC}	V
V_{IH}	Input high voltage (D, C, S)		0.7 V_{CC}	V_{CC} + 1	V
V_{OL}	Output low voltage (Q)	V_{CC} = 5 V, I_{OL} = 2.1 mA		0.4	V
		V_{CC} = 2.5 V, I_{OL} = 100 µA		0.2	V
V_{OH}	Output high voltage (Q)	V_{CC} = 5 V, I_{OH} = –400 µA	0.8 V_{CC}		V
		V_{CC} = 2.5 V, I_{OH} = –100 µA	V_{CC}–0.2		V

Table 18. DC characteristics (M93Cx6-W, device grade 3)

Symbol	Parameter	Test condition	Min.(1)	Max. (1)	Unit
I_{LI}	Input leakage current	$0V \le V_{IN} \le V_{CC}$		±2.5	µA
I_{LO}	Output leakage current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply current (CMOS inputs)	V_{CC} = 5 V, S = V_{IH}, f = 2 MHz, Q = open		2	mA
		V_{CC} = 2.5 V, S = V_{IH}, f = 2 MHz, Q = open		1	mA
I_{CC1}	Supply current (Standby)	V_{CC} = 2.5 V, S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}, pin7 = V_{CC}, V_{SS} or Hi-Z		5	µA
V_{IL}	Input low voltage (D, C, S)		–0.45	0.2 V_{CC}	V
V_{IH}	Input high voltage (D, C, S)		0.7 V_{CC}	V_{CC} + 1	V
V_{OL}	Output low voltage (Q)	V_{CC} = 5 V, I_{OL} = 2.1 mA		0.4	V
		V_{CC} = 2.5 V, I_{OL} = 100 µA		0.2	V
V_{OH}	Output high voltage (Q)	V_{CC} = 5 V, I_{OH} = –400 µA	0.8 V_{CC}		V
		V_{CC} = 2.5 V, I_{OH} = –100 µA	V_{CC}–0.2		V

1. New product: identified by Process Identification letter W or G or S.

Table 19. DC characteristics (M93Cx6-R)

Symbol	Parameter	Test condition	Min.(1)	Max. (1)	Unit
I_{LI}	Input leakage current	$0V \le V_{IN} \le V_{CC}$		±2.5	µA
I_{LO}	Output leakage current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply current (CMOS inputs)	V_{CC} = 5 V, S = V_{IH}, f = 2 MHz, Q = open		2	mA
		V_{CC} = 1.8 V, S = V_{IH}, f = 1 MHz, Q = open		1	mA
I_{CC1}	Supply current (Standby)	V_{CC} = 1.8 V, S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}, pin7 = V_{CC}, V_{SS} or Hi-Z		2	µA
V_{IL}	Input low voltage (D, C, S)		–0.45	0.2 V_{CC}	V
V_{IH}	Input high voltage (D, C, S)		0.8 V_{CC}	V_{CC} + 1	V
V_{OL}	Output low voltage (Q)	V_{CC} = 1.8 V, I_{OL} = 100 µA		0.2	V
V_{OH}	Output high voltage (Q)	V_{CC} = 1.8 V, I_{OH} = –100 µA	V_{CC}–0.2		V

1. This product is under development. For more information, please contact your nearest ST sales office.

Table 20. AC characteristics (M93Cx6, device grade 6 or 3)

Test conditions specified in *Table 12.* and *Table 9.*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SK}	Clock frequency	D.C.	2	MHz
t_{SLCH}		Chip Select low to Clock high	50		ns
t_{SHCH}	t_{CSS}	Chip Select setup time M93C46, M93C56, M93C66	50		ns
		Chip Select setup time M93C76, M93C86	50		ns
t_{SLSH}(1)	t_{CS}	Chip Select low to Chip Select high	200		ns
t_{CHCL}(2)	t_{SKH}	Clock high time	200		ns
t_{CLCH}(2)	t_{SKL}	Clock low time	200		ns
t_{DVCH}	t_{DIS}	Data in setup time	50		ns
t_{CHDX}	t_{DIH}	Data in hold time	50		ns
t_{CLSH}	t_{SKS}	Clock setup time (relative to S)	50		ns
t_{CLSL}	t_{CSH}	Chip Select hold time	0		ns
t_{SHQV}	t_{SV}	Chip Select to READY/$\overline{\text{BUSY}}$ status		200	ns
t_{SLQZ}	t_{DF}	Chip Select low to output Hi-Z		100	ns
t_{CHQL}	t_{PD0}	Delay to output low		200	ns
t_{CHQV}	t_{PD1}	Delay to output valid		200	ns
t_W	t_{WP}	Erase or Write cycle time		5	ms

1. Chip Select Input (S) must be brought low for a minimum of t_{SLSH} between consecutive instruction cycles.
2. $t_{CHCL} + t_{CLCH} \geq 1 / f_C$.

Table 21. AC characteristics (M93Cx6-W, device grade 6)

Test conditions specified in *Table 13.* and *Table 10.*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SK}	Clock frequency	D.C.	2	MHz
t_{SLCH}		Chip Select low to Clock high	50		ns
t_{SHCH}	t_{CSS}	Chip Select setup time	50		ns
t_{SLSH}(1)	t_{CS}	Chip Select low to Chip Select high	200		ns
t_{CHCL}(2)	t_{SKH}	Clock high time	200		ns
t_{CLCH}(2)	t_{SKL}	Clock low time	200		ns
t_{DVCH}	t_{DIS}	Data in setup time	50		ns
t_{CHDX}	t_{DIH}	Data in hold time	50		ns
t_{CLSH}	t_{SKS}	Clock setup time (relative to S)	50		ns
t_{CLSL}	t_{CSH}	Chip Select hold time	0		ns
t_{SHQV}	t_{SV}	Chip Select to READY/$\overline{\text{BUSY}}$ status		200	ns

Table 21. AC characteristics (M93Cx6-W, device grade 6)

Test conditions specified in *Table 13.* and *Table 10.*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
t_{SLQZ}	t_{DF}	Chip Select low to output Hi-Z		100	ns
t_{CHQL}	t_{PD0}	Delay to output low		200	ns
t_{CHQV}	t_{PD1}	Delay to output valid		200	ns
t_W	t_{WP}	Erase or Write cycle time		5	ms

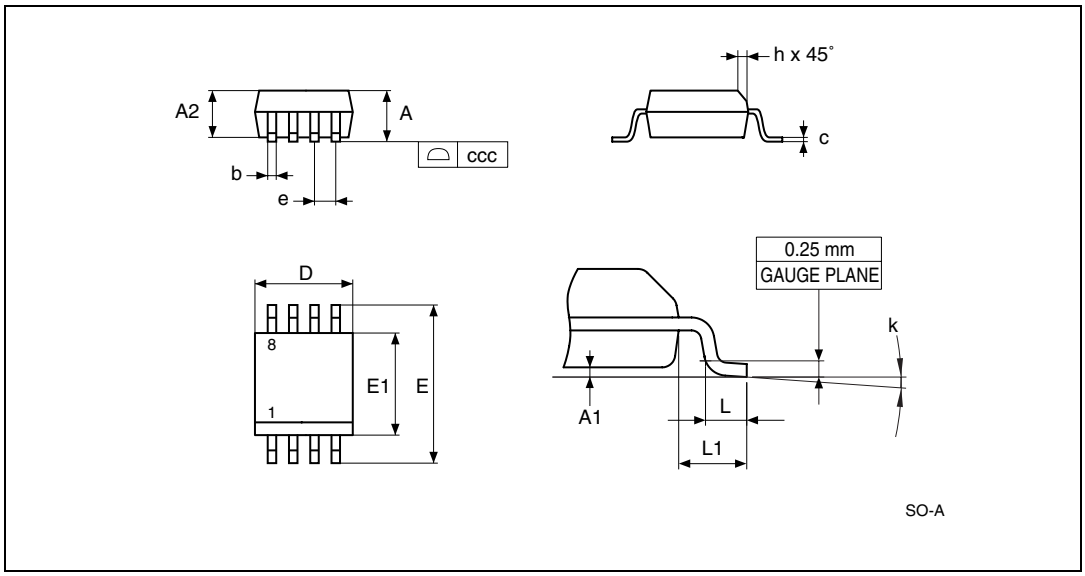
1. Chip Select Input (S) must be brought low for a minimum of t_{SLSH} between consecutive instruction cycles.
2. $t_{CHCL} + t_{CLCH} \geq 1 / f_C$.

Table 22. AC characteristics (M93Cx6-W, device grade 3)

Test conditions specified in *Table 13.* and *Table 10.*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SK}	Clock frequency	D.C.	2	MHz
t_{SLCH}		Chip Select low to Clock high	50		ns
t_{SHCH}	t_{CSS}	Chip Select set-up time	50		ns
t_{SLSH}(1)	t_{CS}	Chip Select low to Chip Select high	200		ns
t_{CHCL}(2)	t_{SKH}	Clock high time	200		ns
t_{CLCH}(2)	t_{SKL}	Clock low time	200		ns
t_{DVCH}	t_{DIS}	Data in set-up time	50		ns
t_{CHDX}	t_{DIH}	Data in hold time	50		ns
t_{CLSH}	t_{SKS}	Clock set-up time (relative to S)	50		ns
t_{CLSL}	t_{CSH}	Chip Select hold time	0		ns
t_{SHQV}	t_{SV}	Chip Select to READY/$\overline{\text{BUSY}}$ status		200	ns
t_{SLQZ}	t_{DF}	Chip Select low to output Hi-Z		100	ns
t_{CHQL}	t_{PD0}	Delay to output low		200	ns
t_{CHQV}	t_{PD1}	Delay to output valid		200	ns
t_W	t_{WP}	Erase or Write cycle time		5	ms

1. Chip Select Input (S) must be brought low for a minimum of t_{SLSH} between consecutive instruction cycles.
2. $t_{CHCL} + t_{CLCH} \geq 1 / f_C$.

Figure 13. SO8 narrow – 8 lead plastic small outline, 150 mils body width, package outline



1. Drawing is not to scale.

Table 25. SO8 narrow – 8 lead plastic small outline, 150 mils body width, package data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A			1.75			0.0689
A1		0.1	0.25		0.0039	0.0098
A2		1.25			0.0492	
b		0.28	0.48		0.011	0.0189
c		0.17	0.23		0.0067	0.0091
ccc			0.1			0.0039
D	4.9	4.8	5	0.1929	0.189	0.1969
E	6	5.8	6.2	0.2362	0.2283	0.2441
E1	3.9	3.8	4	0.1535	0.1496	0.1575
e	1.27	-	-	0.05	-	-
h		0.25	0.5		0.0098	0.0197
k		0°	8°		0°	8°
L		0.4	1.27		0.0157	0.05
L1	1.04			0.0409		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

13 Part numbering

Table 28. Ordering information scheme

Example: M93C86 – W MN 6 T P /S

Device type

M93 = MICROWIRE serial access EEPROM

Device function

86 = 16 Kbit (2048 x 8)
76 = 8 Kbit (1024 x 8)
66 = 4 Kbit (512 x 8)
56 = 2 Kbit (256 x 8)
46 = 1 Kbit (128 x 8)

Operating voltage

blank = V_{CC} = 4.5 to 5.5 V
W = V_{CC} = 2.5 to 5.5 V
R = V_{CC} = 1.8 to 5.5 V

Package

BN = PDIP8
MN = SO8 (150 mils width)
MB = UFDFPN8 (MLP8)
DW = TSSOP8 (169 mils width)

Device grade

6 = Industrial temperature range, –40 to 85 °C.
Device tested with standard test flow
3 = Device tested with high reliability certified flow(1).
Automotive temperature range (–40 to 125 °C)

Packing

blank = standard packing
T = tape and reel packing

Plating technology

P or G = ECOPACK® (RoHS compliant)

Process(2)

/W or /S = F6SP36%

1. ST strongly recommends the use of the Automotive Grade devices for use in an automotive environment. The High Reliability Certified Flow (HRCF) is described in the quality note QNEE9801. Please ask your nearest ST sales office for a copy.
2. Used only for device grade 3.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.